

A Simple ADC Comparison Matrix

Maxim manufactures analog-to-digital converters (ADCs) using the six popular ADC architectures. Deciding on the correct ADC requires tradeoffs between resolution, channel count, power consumption, size, conversion time, static performance, dynamic performance, and price. Designers need to know the key features, and have a basic understanding of the architectures and their design limitations.

This application note provides an overview of the architectures. It includes links to application notes that provide more detail and a handy comparison table that compares the key features and characteristics.

Integrating ADCs

Integrating ADCs provide high resolution and can provide good line frequency and noise rejection. Having started with the ubiquitous ICL7106, these converters have been around for quite some time. The integrating architecture provides a novel yet straightforward approach to converting a low bandwidth analog signal into its digital representation. These type of converters often include built-in drivers for LCD or LED displays and are found in many portable instrument applications, including digital panel meters and digital multi-meters.

[View Specification Table](#)

FLASH ADCs

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. They are suitable for applications requiring very large bandwidths. However, flash converters consume a lot of power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications that typically cannot be addressed any other way. Examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives.

[View Specification Table](#)

Pipelined ADCs

The pipelined analog-to-digital converter (ADC) has become the most popular ADC architecture for sampling rates from a few megasamples per second (MS/s) up to 100MS/s+, with resolutions from 8 to 16 bits. They offer the resolution and sampling rate to cover a wide range of applications, including CCD imaging, ultrasonic medical imaging, digital receiver, base station, digital video (for example, HDTV), xDSL, cable modem, and fast Ethernet.

[View Specification Table](#)

SAR ADC

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are frequently the architecture of choice for medium-to-high-resolution applications, typically with sample rates fewer than 5 megasamples per second (MSPS). SAR ADCs most commonly range in resolution from 8 to 16 bits and provide low power consumption as well as a small form factor. This combination makes them ideal for a wide variety of applications, such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition.

[View Specification Table](#)

Sigma Delta ADC

Sigma Delta analog-to-digital converters (ADCs) are used predominately in lower speed applications requiring a trade off of speed for resolution by oversampling, followed by filtering to reduce noise. 24 bit Sigma Delta converters are common in Audio designs, instrumentation and Sonar. Bandwidths are typically less than 1MHz with a range of 12 to 18 true bits.

[View Specification Table](#)

Two Step ADC

Two Step analog-to-digital converters (ADCs) are also known as subranging converters and sometimes referred to as multi-step or half flash (slower than Flash architecture). This is a cross between a Flash ADC and pipeline ADC and can achieve higher resolution or smaller die size and power for a given resolution are needed vs. a Flash ADC. Example [MAX153](#).

Maxim Application Notes

[Understanding Flash ADCs](#)

[Understanding Integrating ADCs](#)

[Pipeline ADCs Come of Age](#)

[Understanding SAR ADCs](#)

[Demystifying Sigma-Delta ADCs](#)

	FLASH (Parallel)	SAR	DUAL SLOPE (Integrating ADC)	PIPELINE	SIGMA DELTA
Pick This Architecture if you want:	Ultra-High Speed when power consumption not primary concern?	Medium to high resolution (8 to 16bit), 5MSPs and under, low power, small size.	Monitoring DC signals, high resolution, low power consumption, good noise performance ICL7106.	High speeds, few MspS to 100+ MspS, 8 bits to 16 bits, lower power consumption than flash.	High resolution, low to medium speed, no precision external components, simultaneous 50/60Hz rejection, digital filter reduces anti-aliasing requirements.
Conversion Method	N bits - 2^{N-1} Comparators Caps increase by a factor of 2 for each bit.	Binary search algorithm, internal circuitry runs higher speed.	Unknown input voltage is integrated and value compared against known reference value.	Small parallel structure, each stage works on one to a few bits.	Oversampling ADC, 5-Hz - 60Hz rejection programmable data output.
Encoding Method	Thermometer Code Encoding	Successive Approximation	Analog Integration	Digital Correction Logic	Over-Sampling Modulator, Digital Decimation Filter
Disadvantages	Sparkle codes / metastability, high power consumption, large size, expensive.	Speed limited to ~5MSPs. May require anti-aliasing filter.	Slow Conversion rate. High precision external components required to achieve accuracy.	Parallelism increases throughput at the expense of power and latency.	Higher order (4th order or higher) - multibit ADC and multibit feedback DAC.
Conversion Time	Conversion Time does not change with increased resolution.	Increases linearly with increased resolution.	Conversion time doubles with every bit increase in resolution.	Increases linearly with increased resolution.	Tradeoff between data output rate and noise free resolution.
Resolution	Component matching typically limits resolution to 8 bits.	Component matching requirements double with every bit increase in resolution.	Component matching does not increase with increase in resolution.	Component matching requirements double with every bit increase in resolution.	Component matching requirements double with every bit increase in resolution.
Size	2^{N-1} comparators, Die size and power increases exponentially with resolution.	Die increases linearly with increase in resolution.	Core die size will not materially change with increase in resolution.	Die increases linearly with increase in resolution.	Core die size will not materially change with increase in resolution.

MORE INFORMATION

ICL7106: [QuickView](#) -- [Full \(PDF\) Data Sheet \(552k\)](#)

MAX153: [QuickView](#) -- [Full \(PDF\) Data Sheet \(456k\)](#)

-- [Free Sample](#)
-- [Free Sample](#)